**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A method for transmitting data on a bus with minimization of bus switching activity, the method comprising:

converting a datum to be transmitted from its own original format into a transmission format that reduces the bus switching activity, said converting including: swapping a position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern; and selecting, between the sorting patterns, a particular sorting pattern that reduces the bus switching activity upon transmission on the bus of the datum generated using said selected sorting pattern, said selected sorting pattern compressed to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus;

transmitting on at least one line of the bus the datum in said transmission format, and transmitting on one additional line of the bus a synchronization signal having the selected sorting pattern;

receiving the datum in said transmission format, and receiving the synchronization signal having the selected sorting pattern transmitted on the bus; and

converting the datum received from said transmission format to said original format using the selected sorting pattern received, which is decompressed from the $M \cdot \log_2 M$ bits,

wherein a succession of said sorting patterns generated at a transmission end and a succession of sorting patterns generated at a reception end are synchronized with each using a same clock signal supplied to said transmission and reception ends.

2. (Previously Presented) The method according to claim 1 wherein said transmitting on the bus the selected sorting pattern includes:

generating said succession of sorting patterns identifying all possible swaps of the position of the bit or bits of the datum to be transmitted;

comparing the particular sorting pattern to be transmitted with the sorting patterns generated; and

generating and transmitting on the bus said synchronization signal upon detection of a coincidence between the particular sorting pattern to be transmitted and one of the sorting patterns generated .

3. (Previously Presented) The method according to claim 2 wherein said receiving the selected sorting pattern transmitted on the bus includes:

generating said succession of sorting patterns identical to, and synchronous with, the generated succession of sorting patterns identifying all possible swaps of the position of the bit or bits of the datum to be transmitted; and

identifying one of the succession of sorting patterns that is generated at an instant of reception of the synchronization signal transmitted on the bus, the sorting pattern identified being identical to said selected sorting pattern to be transmitted.

4. (Previously Presented) The method according to claim 3 wherein the sorting pattern selected reduces the bus switching activity to a minimum amount.

5. (Previously Presented) The method according to claim 2 wherein said generating the succession of sorting patterns includes :

providing a finite state machine having a number of internal states equal to a number of possible swaps of the position of the bit or bits of the datum to be transmitted;

associating to each of the internal states of said finite state machine a respective sorting pattern; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate said sorting patterns,

wherein said same clock signal supplied to said transmission and reception ends is respectively supplied to said finite state machine and to another finite state machine at said reception end.

6. (Previously Presented) The method according to claim 2 wherein said generating the succession of sorting patterns includes:

generating a plurality of disjoint sets of sorting patterns, each set being formed by a sorting pattern identifying a respective subset of possible swaps of the position of the bit or bits of the datum to be transmitted, the sorting patterns of each set being further generated in succession and in a synchronous way with respect to the sorting patterns of the other sets.

7. (Previously Presented) The method according to claim 6 wherein the generating the plurality of separate sets of sorting patterns includes, for each said set of sorting patterns:

providing a finite state machine having a number of internal states equal to a number of sorting patterns in the set;

associating to each of the internal states of said finite state machine a respective sorting pattern; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding sorting patterns,

wherein said same clock signal supplied to said transmission and reception ends is respectively supplied to said finite state machine and to another finite state machine at said reception end.

8. (Currently Amended) A system for transmitting data on a bus with minimization of bus switching activity, the device comprising:

first converting means for converting a datum to be transmitted from its own original format to a transmission format that minimizes the bus switching activity, said first converter means including:

a swap operator for swapping a position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern; and

selecting means for selecting, between the various sorting patterns, an optimal sorting pattern that minimizes the bus switching activity upon transmission on the bus of the datum generated using said optimal sorting pattern;

a compression module that compresses said selected optimal pattern to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus;

transmitting means for transmitting on at least one line of the bus the datum in said transmission format and on one additional line of the bus a synchronization signal having the optimal sorting pattern;

receiving means for receiving the datum in said transmission format and said optimal sorting pattern transmitted on the bus, the receiving means including a decompression module to decompress the optimal sorting pattern; and

second converting means for converting the datum received from said transmission format to said original format using said optimal sorting pattern received,

wherein said transmitting means includes:

first sorting pattern generating means for generating a succession of sorting patterns identifying all possible swaps of the position of the bit or bits of the datum to be transmitted;

comparing means for comparing the optimal sorting pattern to be transmitted with the sorting patterns generated;

signal generating means for generating and sending onto said additional line of said bus said synchronization signal upon detection of an identity between the optimal sorting pattern to be transmitted and one of the sorting patterns generated,

wherein said receiving means includes:

second sorting pattern generating means for generating a succession of sorting patterns identical to, and synchronous with, the sorting patterns generated by said first sorting pattern generating means; and

detecting means for identifying one of the sorting patterns generated by said second sorting pattern generating means at an instant of reception of the synchronization signal transmitted on the bus, the sorting pattern identified being identical to said optimal sorting pattern to be transmitted,

wherein said succession of said sorting patterns generated at transmission and said succession of sorting patterns generated at reception are synchronized with each other using a same clock signal supplied to said transmitting means and to said receiving means.

9. (Previously Presented) The system according to claim 8 wherein said first and second sorting pattern generating means each include a finite state machine, supplied with said same clock signal, having a number of internal states equal to a number of possible swaps of the position of the bit or bits of the datum to be transmitted, a respective sorting pattern being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

10. (Previously Presented) The system according to claim 8 wherein said first and second sorting pattern generating means each include a plurality of sorting pattern modules generating a plurality of disjoint sets of sorting patterns, each set being formed by a sorting pattern identifying a respective subset of all the possible swaps of the position of the bit or bits of the datum to be transmitted, the sorting patterns of each set being further generated in succession and in a synchronous way with respect to the sorting patterns of other sets.

11. (Previously Presented) The system according to claim 10 wherein each of said sorting pattern generating modules includes a finite state machine, supplied with said same clock signal, having a number of internal states equal to a number of sorting patterns of the corresponding set, a respective sorting pattern being associated to each of the internal states of said finite state machine, said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate said sorting patterns.

12. (Currently Amended) A computer product loadable into a memory associated with a bus, said computer product having portions of software code that are executable by a processor to minimize bus switching activity, by:

converting a datum to be transmitted from its own original format into a transmission format that reduces the bus switching activity, said converting including: swapping a position of one or more bits of the datum to be transmitted, said swapping being performable according to a plurality of different variants, each of which is identified by a respective sorting pattern; and selecting, between the sorting patterns, a particular sorting pattern that reduces the bus switching activity upon transmission on the bus of the datum generated using said selected sorting pattern, and compressing said selected sorting pattern to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus;

transmitting on at least one line of the bus the datum in said transmission format; and

transmitting on one additional line of the bus a synchronization signal having said selected sorting pattern and usable by a receiving device to identify said selected sorting pattern from a plurality of sorting patterns, which is decompressed from the $M \cdot \log_2 M$ bits,

wherein a succession of said sorting patterns generated at a transmission end and a succession of sorting patterns generated at a reception end are synchronized with each using a same clock signal supplied to said transmission and reception ends.

13. (Currently Amended) A method for communicating *n*-bit data on a single line, comprising:

in transmission:

generating in succession all possible combinations of *n* bits;

comparing an *n*-bit datum to be transmitted with the combinations of *n* bits generated; and

generating and transmitting ~~on said single line~~ an identity signal, upon detection of a coincidence between the *n*-bit datum to be transmitted and one of the combinations of *n* bits generated in accordance with a selected sorting pattern, compressing said selected sorting pattern to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus, and further generating and transmitting ~~in addition to said identity signal~~ on the single line at least one signal that transmits said data; and

in reception:

generating a succession of combinations of *n* bits identical and synchronous to the combinations generated in succession in transmission; and

identifying one of the combination of *n* bits generated at an instant of reception of the identity signal ~~transmitted on the single line~~in accordance with the selected sorting pattern, which is decompressed from the $M \cdot \log_2 M$ bits, the combination of *n* bits identified corresponding to the *n*-bit datum to be transmitted,

wherein said succession of combinations generated at transmission and said succession of combinations generated at reception are synchronized with each other using a same clock signal supplied at said transmission and at said reception.

14. (Previously Presented) The method according to claim 13 wherein said generating in succession all the possible combinations of *n* bits in said transmission and in said reception includes:

providing a finite state machine, supplied with said same clock signal, having a number of internal states equal to a number of possible combinations of *n* bits;

associating to each of the internal states of said finite state machine a respective combination of *n* bits; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

15. (Previously Presented) The method according to claim 13 wherein said generating the combinations of *n* bits in said transmission and in said reception includes:

generating a plurality of disjoint sets of possible combinations of *n* bits, the combinations of *n* bits of each set being further generated in succession and in a synchronous way with respect to the combinations of *n* bits of the other sets.

16. (Previously Presented) The method according to claim 15 wherein the generating a plurality of disjoint sets of possible combinations of *n* bits in said transmission and in said reception includes, for each said set of combinations of *n* bits:

providing a finite state machine, supplied with said same clock signal, having a number of internal states equal to a number of combinations of *n* bits in the set;

associating to each of the internal states of said finite state machine a respective combination of *n* bits; and

operating said finite state machine at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

17. (Currently Amended) A system for transmitting *n*-bit data on a single line in a bus, comprising:

at a transmission end:

first combination generating means for generating in succession all possible combinations of *n* bits;

comparing means for comparing an *n*-bit datum to be transmitted with the combinations of *n* bits generated; and

signal generating means for generating and transmitting on said single line an identity signal, upon detection of a coincidence between the *n*-bit datum to be transmitted and one of the combinations of *n* bits generated in accordance with a sorting pattern, said signal generating means further generating and transmitting ~~in addition to said identity signal~~ on the single line at least one signal that transmits said data, a compression module that compresses said sorting pattern to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus; and

at a reception end:

second combination generating means for generating a same succession of combinations of *n* bits as that generated by the first combination generating means, the successions of combinations of *n* bits generated by the said first and second combination-generating means being synchronized with one another; and

detecting means for identifying one of the combination of *n* bits generated by said second combination generating means at an instant of reception of the identity signal transmitted ~~on the single line~~, the combination of *n* bits identified corresponding to the *n*-bit datum to be transmitted,

wherein said succession of combinations generated at said transmission end and said succession of combinations generated at said reception end are synchronized with each other using a same clock signal supplied to said transmission end and to said reception end.

18. (Previously Presented) The system according to claim 17 wherein each of said first and second combination generating means include a finite state machine, supplied with said same clock signal, having a number of internal states equal to a number of possible combinations of *n* bits, a respective combination of *n* bits being associated to each of the internal states of said finite state machine, and said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

19. (Previously Presented) The system according to claim 17 wherein said first and second combination generating means each include a plurality of combination generating modules generating a plurality of disjoint sets of possible combinations of *n* bits, the combinations of *n* bits of each set being generated in succession and in a synchronous way with respect to the combinations of *n* bits of the other sets.

20. (Previously Presented) The system according to claim 19 wherein each of said combination generating modules includes a finite state machine, supplied with said same clock signal, having a number of internal states equal to a number of combinations of *n* bits in the set, a respective combination of *n* bits being associated to each of the internal states of said finite state machine, and said finite state machine being operated at a given frequency so as to cause its internal state to evolve and generate the corresponding combinations of *n* bits.

21. (Previously Presented) A computer product loadable into a memory , said computer product including portions of software code that can implement the method according to claim 13 when the computer product is executed by a digital processor associated to the bus.

22. (Currently Amended) A transmitter device coupled to a bus, comprising:

a converter to convert a datum to be transmitted, on at least one line of the bus, from an initial format to a transmission format, said transmission format being a selected sorting pattern from among a succession of sorting patterns that identify possible swaps of bit positions of said datum; and

a first finite state machine having a number of internal states equal to a number of said sorting patterns and each of said internal states respectively corresponding to one of said sorting patterns;

wherein said first finite state machine is adapted to be supplied with a clock signal to synchronize each internal state of said first finite state machine with a respective same internal state of a second finite state machine, at a receiving end, that is also supplied with same said clock signal and that receives said datum in said transmission format and that also has a number

of internal states equal to said number of said sorting patterns and each of said internal states of said second finite state machine at the receiving end also respectively corresponding to one of said sorting patterns, a compression module that compresses said corresponding sorting pattern to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus,

wherein said first finite state machine is adapted to generate a synchronization signal sent on one additional line of said bus to be received by said second state machine, said synchronization signal corresponding to a particular one of said internal states of said first finite state machine that corresponds to said selected sorting pattern used in transmission of said datum and said synchronization signal being adapted to be used by said second finite state machine to identify said selected sorting pattern including a decompression module that decompresses the optimal sorting pattern from a particular one of said internal states of said second state machine that is synchronized by said clock signal with said particular internal state of said first finite state machine.

23. (Previously Presented) The device of claim 22, further comprising a register to store said sorting patterns.

24. (Previously Presented) The device of claim 22 wherein said sorting patterns are from among a plurality of disjoint sets of sorting patterns.

25. (Cancelled)